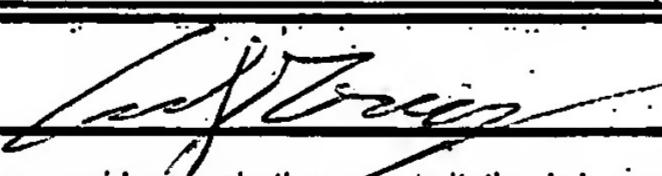


Substitute for form 1449A/PTO		<b>Complete If Known</b>		
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>		Application Number	10023394	
(Use as many sheets as necessary)		Filing Date		
		First Named Inventor	Pan, Phillip	
		Art Unit		
		Examiner Name		
Sheet	1	of	2	Attorney Docket Number
015114-054411US				

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number Number Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
AT	AA	US-5,555,214	09-10-1996	Sung et al.	
	AB	US-5,633,830	05-27-1997	Sung et al.	05-27-1997
	AC	US-5,764,080	09-01-1998	Huang et al.	06-09-1998
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	AN	US-6,100,713	08-08-0000	Kalb et al.	Aug. 8, 2000
	AO	US-6,147,520	11-14-00	Kothandaraman et al.	Nov. 14, 2000
	AP				
	AQ				
	AR				
	AS				
	AT				

FOREIGN PATENT DOCUMENTS							
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup>	Number <sup>4</sup>				
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	BB						<input type="checkbox"/>

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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Sheet

2

of 2

**Complete If Known**

Application Number

10623394

Filing Date

First Named Inventor

Pan, Phillip

Art Unit

Examiner Name

Attorney Docket Number

015114-054411US

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
AJ	BC	MICHAEL B. BENDAK et al., "CMOS VLSI Implementation of Gigabyte/Second Computer Network Links", IEEE, 1996	
	BD	"Virtex-II 1.5V Field-Programmable Gate Arrays", XILINX, DS031-2 (v1.5), April 2, 2001	
	BE	ANDREA BONI et al., "LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-μm CMOS" IEEE Journal of Solid-State Circuits, vol. 36, no. 4, April 2001	
	BF	"APEX II Programmable Logic Device Family", Altera Corporation, May 2001	
	BG	"APEX 20K Programmable Logic Device Family", Altera Corporation, May 2001	
	BH	LVDS I/O Interface for Gb/s-per-Pin Operation in 0.35-μm CMOS; Boni, et al., IEEE Journal of Solid-State Circuits, Vol. 36, No. 4, April 2001	
	BI	CMOS VLSI Implementation of Gigabyte/Second Computer Network Links, Bendak et al., Dept. of Electrical and Computer Engineering, University of California at San Diego, La Jolla, CA 92093-0407, IEEE International Symposium on Circuits and Systems, 1996	
	BJ	APEX II Programmable Logic Device Family, A-DS-APEXII-1.1, ver. 1.1, May 2001, Altera Corporation, San Jose, CA	
	BK	APEX 20K Programmable Logic Device Family, A-DS-APEX20K-03.7, ver. 3.7, May 2001, Altera Corporation, San Jose, CA	
→	BL	Virtex-II 1.5V Field-Programmable Gate Arrays, DS031-2 (v1.5), April 2, 2001, Xilinx, Incorporated, San Jose, CA	
	BM		

Examiner Signature:

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of 1

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Application Number	10/623,394
Filing Date	July 18, 2003
First Named Inventor	Pan, Phillip
Art Unit	
Examiner Name	
Attorney Docket Number	015114-054411US

### U.S. PATENT DOCUMENTS+

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code <sup>2</sup> (if known)			
AJ	AA	US-6,278,073 B1	08/21/01	McCracken et al.	
	AB	US-6,472,904 B2	10/29/02	Andrews et al.	
	AC	US-6,504,790 B1	01/07/03	Wolford	
	AD	US-			
	AE	US-			
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### FOREIGN PATENT DOCUMENTS

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		Country Code <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)				
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Signature*Phillip Pan*Date  
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